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INSTRUCTION MANUAL

SIDEREAL RATE GENERATOR AND CLOCK

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GREENBELT, MARYLAND

INSTRUCTION MANUAL

SIDEREAL RATE GENERATOR

AND CLOCK

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NETWORK ENGINEERING BRANCH

NETWORK ENGINEERING AND OPERATIONS DIVISION

Patent Pending

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SECTION 1

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

This manual provides a comprehensive technical description of the operating and physical characteristics of the sidereal rate generator (Fig. 1.1). It outlines maintenance procedures and provides sufficient information concerning the functional theory of operation to permit intelligent and effective operation and maintenance of the unit.

1.2 SYSTEM CONCEPT

The sidereal rate generator generates a time scale that utilizes as its reference the relative position of the stars with respect to the rotation of the earth. The sidereal rate generator therefore provides the means for directly comparing long-term data with sidereal time.

The sidereal rate generator provides output pulses or ticks whose phase can be manually controlled with the calibrated front-panel time-reference control. Auxiliary variable-phase outputs of 1-PPS ticks for oscilloscope triggering and a 1-kc variable-phase sine wave are also available.

1.3 SIDEREAL TIME

A sidereal day is defined as the interval between two successive transits of the first point of Aries over the upper meridian of any one point. The sidereal day contains 24 sidereal hours each having 60 sidereal minutes of 60 sidereal seconds. In mean solar time, the sidereal day is 23 hours, 56 minutes, and 4.09 seconds. The difference in time between the mean solar day and the sidereal day is due to the earth's motion about the sun and the influence of the motion on the apparent position of the earth among the stars.

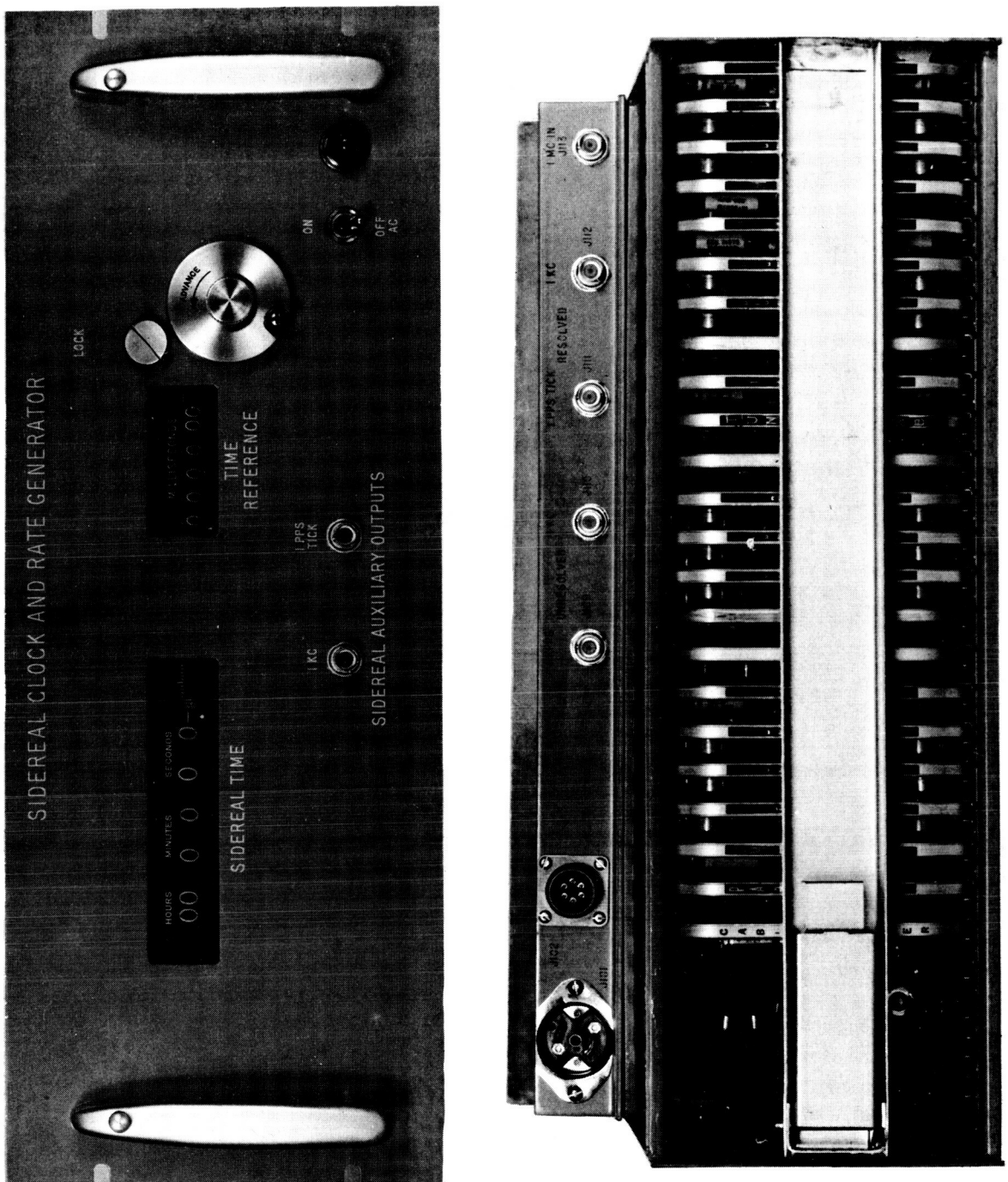


FIGURE 1.1 - SIDEREAL RATE GENERATOR

What happens is that, during the course of the day, the earth's orbital motion causes the sun to appear to move a little to the east among the stars. Even if the earth did not rotate, the sun would appear to move eastward completely around the earth during one period of the earth's orbit. The effect of this apparent motion is that the day referenced to the sun is about 4 minutes longer than the day referenced to the stars. For this reason a solar year will contain 366.24+ sidereal days or 1 more than the number of mean solar days. This solar unit is an aid for following or tracking star positions and checking angle data with star references.

SECTION 2

OPERATING INSTRUCTIONS

2.1 GENERAL

This section describes the installation, turn-on procedures, and system operational checks for the sidereal rate generator.

2.2 UNPACKING AND INSPECTION

Inspect the sidereal rate generator for damage as soon as it is received. Check for broken knobs or broken connectors and inspect the cabinet and panel surfaces for dents and scratches.

2.3 INSTALLATION

Mount the sidereal rate generator in a standard 19-inch equipment rack. Ambient temperature in the rack during normal operation should not exceed a maximum of 50°C or a minimum of 0°C.

Connect the sidereal rate generator to a 115-volt, single-phase 60-cps power source. The accurate specifications for the system are met for line voltages from 105 to 125 volts and frequencies from 55 to 65 cps.

Turn the Dressen Barns power supply to the "ON" position and set it to 20-volts dc; however, the sidereal rate generator should continue to operate without gaining or losing time even if the power supply varies between 18 and 20 volts.

Connect an accurate and stable 1-Mc oscillator to the 1-Mc input (J113) at the rear of the cabinet. Turn the RP-31 power supply to the "ON" position, and then turn the +12-, -6-, and -18-volt circuit breakers to the "ON" position; power is now supplied to the sidereal rate generator.

The sidereal rate generator is now ready for use. Output connections from the sidereal rate generator can be made at any time.

2.4 PERFORMANCE TEST

Because of its fail-safe circuit design the clock mechanism either operates properly or stops completely. Allow a 30-second warmup before proceeding as follows:

2.5 SIDEREAL-RATE-GENERATOR OUTPUTS

Connect the sidereal rate generator to an oscilloscope and measure the outputs on the oscilloscope. Check the unresolved sidereal 1-kc output on the counter to insure that the output is 1.002+kc. The wave-form data are shown in TABLE 2.1.

TABLE 2.1

SIDEREAL-RATE-GENERATOR OUTPUT WAVE FORMS

Clock outputs	Signal	Amplitude (peak-to-peak)	Card Number	Pin Number	Jack No.
1-KPPS unresolved	square	6v(3c Logic)	22	8	J109
1-kc unresolved	sine	3 v	23	24	J110
1-kc resolved	sine	2 v	front panel		J107
1-kc resolved	sine	2 v	rear panel		J112
1-PPS tick	tick	-10 v	front panel		J108
1-PPS tick	tick	+10 v	rear panel		J111

2.6 OPERATING CONTROLS

Refer to Figure 2.1 and Table 2.2 for description and explanation of the operating controls. The control number in the table refers to the control number shown in the figure.

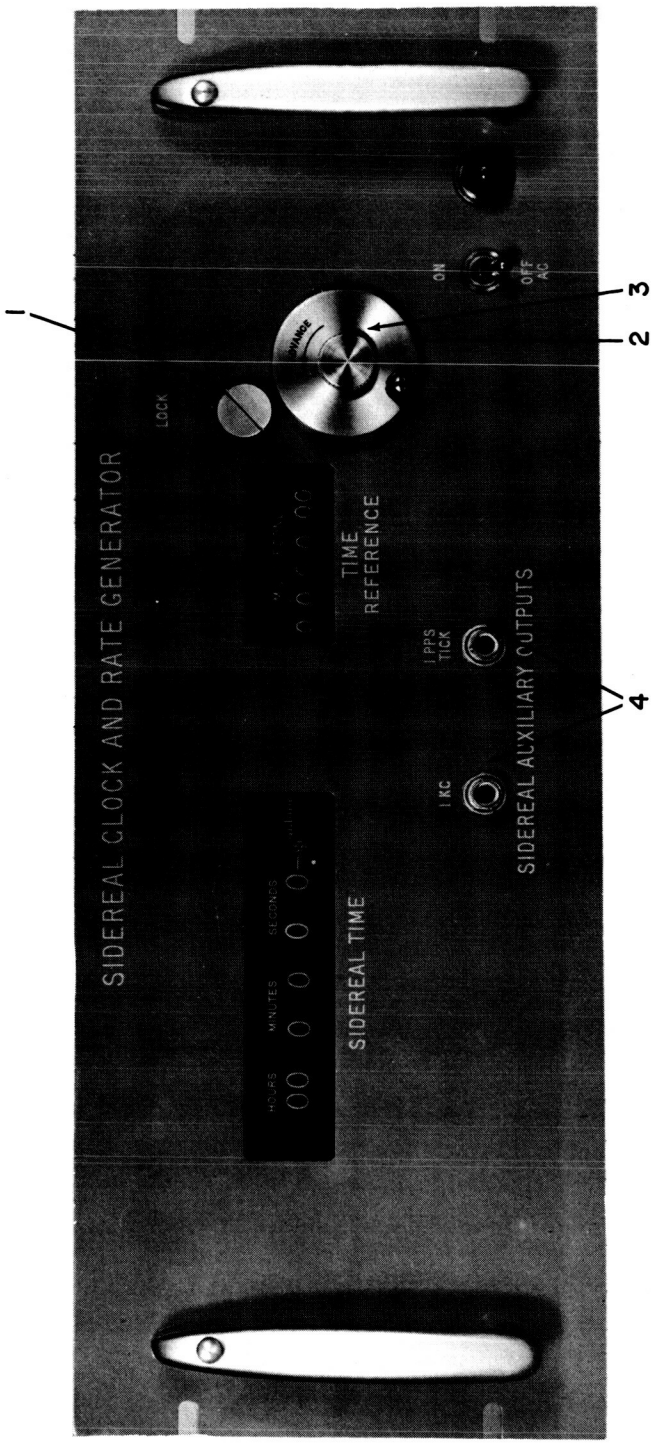


FIGURE 2.1 FRONT-PANEL CONTROLS

TABLE 2.2

OPERATING CONTROLS

Control number	Name	Function
1	Lock	Holds time-reference control setting; keep tightened to prevent inadvertent changing of setting.
2	Time-reference control	This control shifts phase of the 1-PPS TICKS, AUXILIARY PULSE, and 1-kc resolved sine-wave outputs. Counter-clockwise rotation (in the direction of the ADVANCE arrow) shifts the TICKS, the AUXILIARY PULSE, and the 1-kc pip outputs behind time.
3	Vernier dial	One full rotation of the vernier dial is equivalent to a time shift of 1,000 microseconds or 1 millisecond and changes the MILLISECONDS indicator by one count.
4	Auxiliary outputs	The auxiliary outputs provide a 1-PPS TICK for the oscilloscope trigger and a 1-kc sine-wave signal.

2.7 ALINEMENT OF THE RESOLVER

The alinement of the resolver can be checked as follows:

1. Trigger oscilloscope with the unresolved phase-shifted 1-PPS signal.

2. Connect the oscilloscope probe to observe the 1-kc sine wave at the 1-kc unresolved output (J110 rear panel).

3. Set the time-reference control to 000.00 millisecond.

4. Set the time per cm to 0.1 MS/CM (1-ms full scale).

5. Position oscilloscope trace to place positive peaks of the 1-kc sine wave on the vertical centerline of the CRT.

6. Turn the time-reference control, noting both oscilloscope presentation and millisecond dial reading. One cycle should move pass the vertical centerline for each 1.00-millisecond dial division.

2.8 HOURS, MINUTES, AND SECONDS ADJUSTMENT

The clock can be set manually in 1-hour, 1-minute, and 1-second increments, or it can be adjusted electrically in 10-microsecond increments. Hours and minutes drums must be adjusted with the clock stopped. Seconds drums are adjusted with the clock operating. To set the clock, proceed as follows:

1. Slide chassis partly out of the cabinet.

2. Pull out spring-loaded pin at left side of clock mechanism. Turn knurled wheel (located at the left side of the hours drum) in either direction until the seconds drum is at any number between 10 and 49.

3. Slide minutes-adjust block (located behind and to the right of the unit minute drum) to the left (as viewed from the front panel). Turn the minutes drum in any direction to any reading between 10 and 49.

4. Slide hours-adjust block (located behind and to the right

of the hours drum) to the left (as viewed from the front panel). Turn hours drum to either direction until desired hour reading is centered in the window.

5. Reset minutes drum (see step 3) to the desired minute reading. Turn minutes drum in either direction without passing 00 minute until desired reading is centered in the window (passing 00 will disturb hour setting).

6. To start the clock motor the starting knob, which is located on the right side of the clock mechanism (as viewed from the front panel), must be spun at or above its synchronous speed (the normal operating speed of a synchronous motor). Indications of sub-synchronous starting speed are high motor noise and slow movement of the clock dial.

7. Reset seconds drum (see step 2) to the desired seconds reading. Spring-loaded pin must drop into hole on adjustment wheel when pin is released. Each position hole on the wheel is equivalent to 1 second.

2.9 THE 1-RPS INDICATOR DRUM

The 1-RPS indicator drum is controlled by the signal driving the clock motor and is synchronized with the tick output pulse. Manually advancing or retarding the time-reference vernier control by one revolution adds or subtracts 1 millisecond from the 1-PPS TICK output.

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The theory of operation of the sidereal rate generator is presented in this section. Some of the units used are standard items. The detailed theory of operation of the S-PAC digital modules used in the sidereal rate generator can be found in the Instruction Manual for S-PAC Digital Modules, Computer Control Co., Inc. A detailed description of the clock mechanism can be found in the Operating and Service Manual, 115 BR Frequency Divider and Digital Clock, Hewlett-Packard Co.

The theory contained herein applies only to the units designed specifically for use by the sidereal rate generator, except where information on the standard items is necessary for a complete understanding of the operation of the sidereal rate generator.

A clock keeping time in sidereal units must, in the course of a year, indicate the passage of one day more than it would in mean solar units. In other words, the ratio of sidereal units to the units of mean solar time must be 366.24^{+} to 365.24^{+}. This means that a clock which indicates mean solar time when driven at a 1-kc rate will indicate sidereal time when driven at a 1.00273792-kc rate. The problem is to develop this 1.002^{+} kc rate for driving clocks and astronomical tracking devices from sources of standard UT2 frequencies such as 1 Mc which can be easily checked and compared with many other sources.

The ratio of mean solar units to sidereal units is 0.997269566. This ratio has been ascertained to nine places. The number 0.9972695680 was used in the sidereal rate generator because of its ability to be factored in a suitable fashion; this ratio results in a sidereal rate accurate to two digits in the eighth place.

If 1 Mc is divided by 997.2695680, 1.002^{+} kc will result. The value 997.2695680 was broken down into its factors of $41 \times 83 \times 19 \times 241 \times 0.2^{6}$ or $41 \times 83 \times 19 \times 241 / 5^{6}$ for ease of division.

The main functional sections and the signal flow within the sidereal rate generator is shown in the operational block diagram of Figure 3.1.

3.2 BLOCK-DIAGRAM DESCRIPTION OF DIVIDER CHAIN

The divider chain is shown in the functional block diagram of Figure 3.2 and the block diagram of Figure 3.3. The divider chain performs the multiplications and divisions necessary to render the sidereal rate of 1.002^{+} kc from the 1-Mc input frequency.

The multiplications by 5 are performed by tuned filters designed to remove the fifth harmonic of their respective inputs and tuned amplifiers which amplify the resulting fifth harmonic signal. Amplification by a tuned amplifier is necessary to reduce the jitter and ripple and results in a more stable output. The divisions are performed by binary dividers. The series of division and multiplication operations was selected so that frequencies at which tank circuits could be effectively constructed using readily available components would result.

Since 1-Mc logic binaries are used in the present system, the 1-Mc input could not be divided by 41 because of the propagation delay of the carry pulse through the circuits of the divider chain. Instead, the 1-Mc signal is first divided by 2 and then by 41 to allow for the delay; a frequency-doubler circuit and a tuned amplifier circuit is utilized later in the divider chain to compensate for the extra division by 2.

The highly accurate and stable 1-Mc signal is applied to a Schmitt trigger circuit where it is converted to a rectangular wave compatible with the binaries used in the divider chain. The rectangular 1-Mc output from the Schmitt trigger is applied to eight

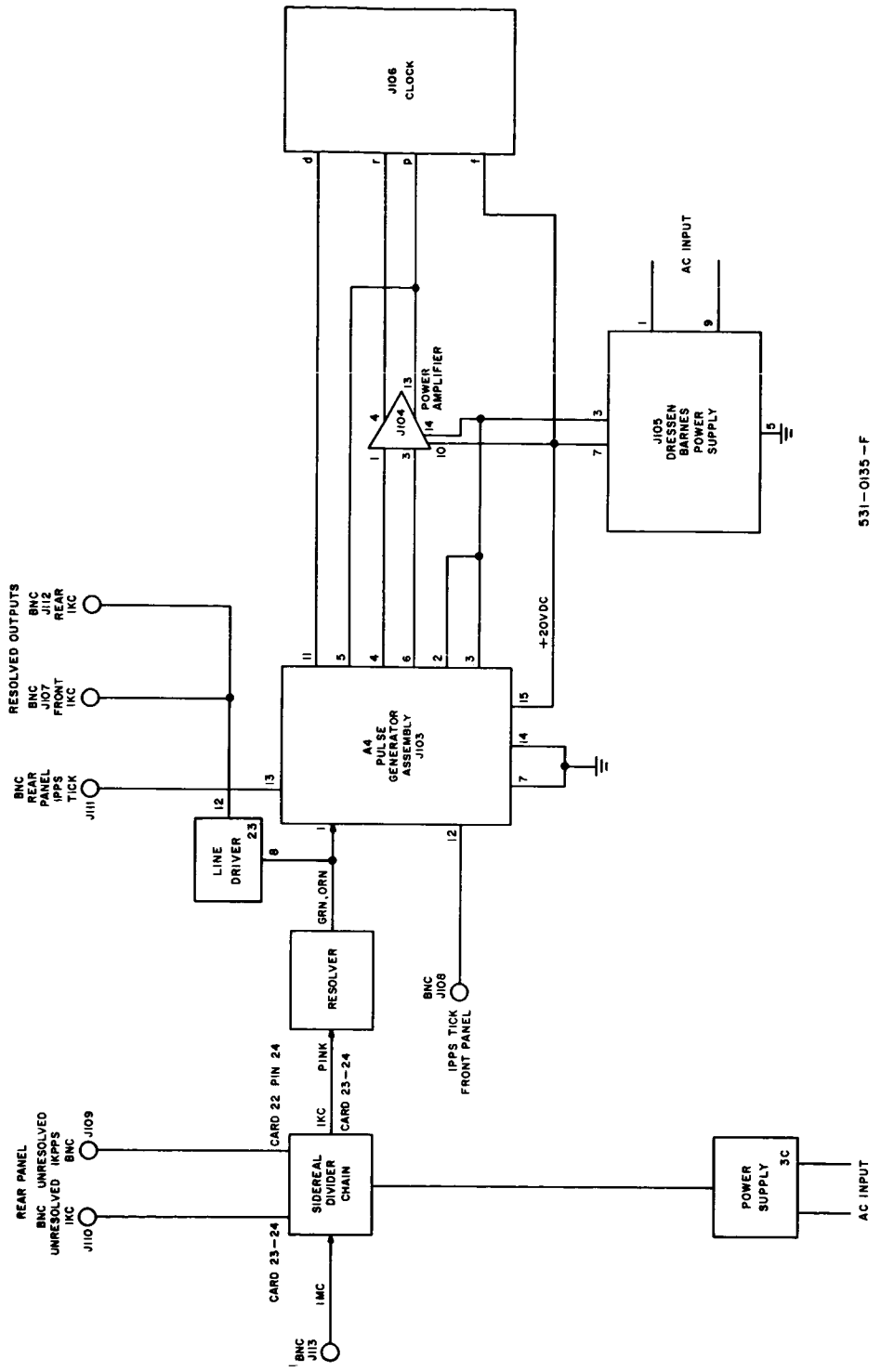


FIGURE 3.1- SIDEREAL RATE GENERATOR, OPERATIONAL BLOCK DIAGRAM

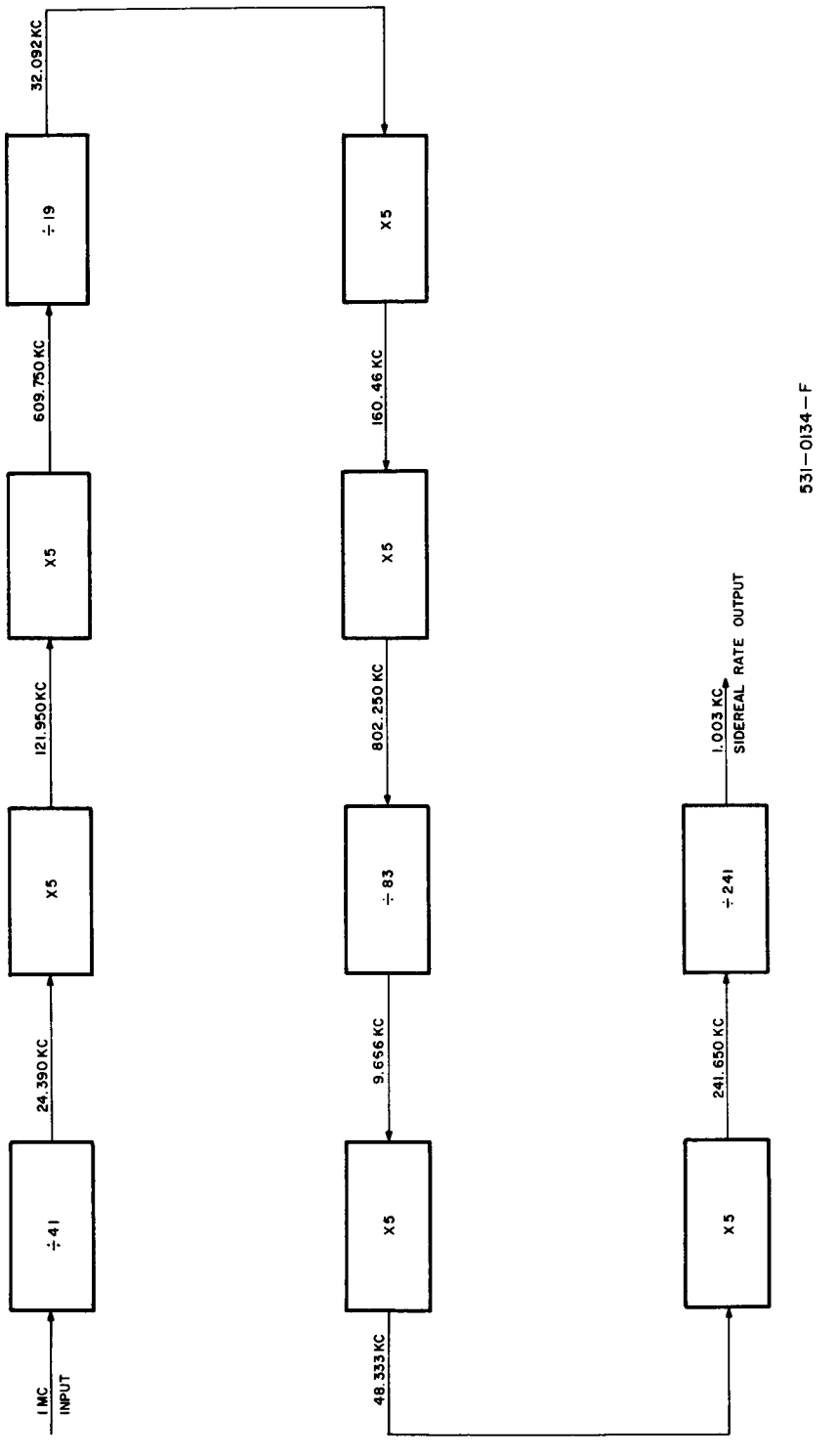


FIGURE 3.2 - DIVIDER CHAIN, FUNCTIONAL BLOCK DIAGRAM

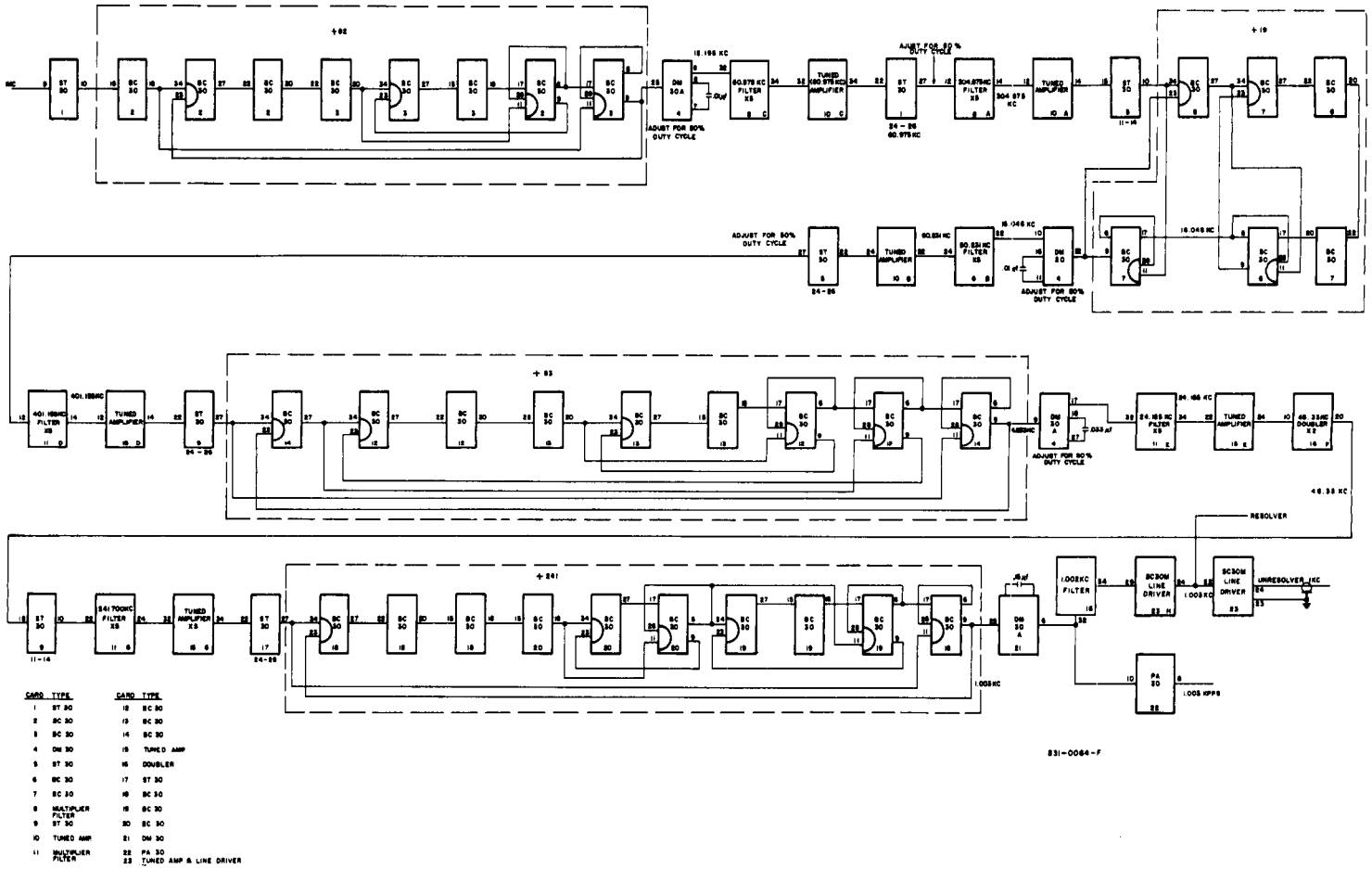


FIGURE 3.3-DIVIDER CHAIN, OPERATIONAL BLOCK DIAGRAM

cascaded binary counters connected in a divide-by-82 configuration. The output from the divide-by-82 circuit which is a 12.195-KPPS signal is applied through a delay multivibrator for pulse-width shaping to a filter circuit tuned to resonate at the fifth harmonic of the input frequency. This in effect multiplies the 12.195-KPPS signal by five and produces a 60.955-kc sine wave. The 60.955-kc sine wave is applied to a tuned amplifier which resonates at the input frequency, in this case 60.955 kc. The tuned amplifier reduces the jitter and ripple and produces a very stable output signal.

The process of multiplication and division is continued until the desired 1.002-kc sidereal rate is obtained, as shown in Figures 3.2 and 3.3.

3.3 EIGHT BINARIES CONNECTED IN A DIVIDE-BY-82 CONFIGURATION

Eight binaries connected in a divide-by-82 configuration are shown in Figure 3.4. In the diagram at the bottom of the figure the waveforms are the dc potentials at the output from each binary. Waveforms are oriented in relation to the frequency applied to the input.

Reading from left to right, each up-going line is a positive-going pulse (in this case, from -6v to ground) which causes a binary to change its state. Each down-going line (from ground to -6v) has no effect on the binary. As shown, one output is obtained after 82 input pulses.

In the following discussion it is assumed that initially all binaries are in the "Zero" state. That is, the true outputs from each binary are at ground potential (zero volt).

The second and fifth binary stages have a gated complement input. When either of the inputs are at "one" (-6v) the gate is enabled and a positive transition at the other input will cause the binary to change its state. However, when any of the inputs are at "zero"

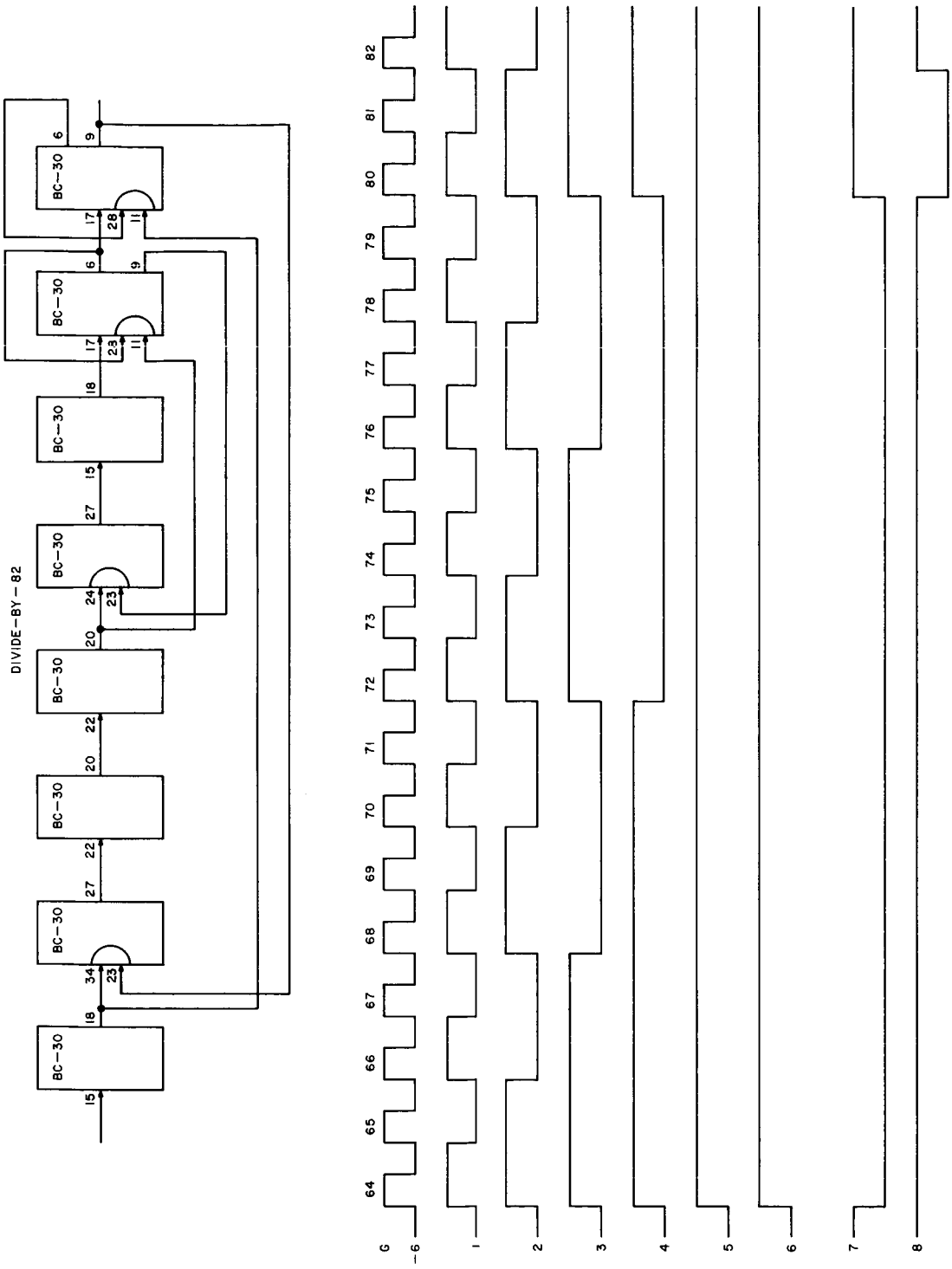


FIGURE 3.4 - EIGHT BINARIES CONNECTED IN A DIVIDE-BY-82 CONFIGURATION

(ground potential) the gate is inhibited and a positive transition at the other input has no effect on the binary. The seventh and eighth binaries have gated ac reset inputs. A positive transition applied to either input when the binary is in the set (zero) state resets the binary to the one state.

The binaries are connected in the following manner: The output from pin 18 of the first binary is utilized as one of the gate inputs to both the second and eighth binary. The other gate input to the second binary is the output from pin 9 (reset output) of the eighth binary. The output from pin 6 (set output) from the eighth binary is fed back as the other gate input to the eighth binary. The output from pin 20 of the fourth binary is utilized as one of the gate inputs to both the fifth and seventh binaries. The other gate input to the fifth binary is the output from pin 9 (reset output) from the seventh binary. The output from pin 6 (set output) from the seventh binary is fed back as the other gate input to the seventh binary.

The first 64 input pulses cause the circuit to operate as a straight binary counter. The 64th pulse, however, causes the seventh binary to change its state. The output from pin 9 which was at "one" (-6 v) now becomes a "zero" (0 v) inhibiting the input to the fifth binary. The output from pin 6 of the seventh binary, which was at "zero" (0 v), now becomes a "one" (-6 v) enabling the gated input to the seventh binary.

The 72nd input pulse will cause the fourth binary to change its state again. The output from pin 20 of the fourth binary, which is a negative transition, will have no effect on the other binaries.

The 80th input pulse will cause the fourth binary to change its state again. The output from pin 20 of the fourth binary, which is a positive transition, will have no effect on the fifth binary because the input gate is inhibited. The positive transition, however, will cause the seventh binary to change its state. The positive transition occurring at the output (pin 6) of the seventh binary will cause the eighth binary to change its state.

The 81st input pulse will cause the first binary to change its state again. The output from the first binary (pin 18), which is a negative transition, will have no effect on the other binaries.

The 82nd input pulse will cause the first binary to change its state once more. The positive transition occurring at the output of the first binary (pin 18) will have no effect on the second binary because the input gate is inhibited. This positive transition, however, will cause the eighth binary to change its state again. Therefore, one output pulse will be obtained for every 82 input pulses. The 1-Mc input signal has been, in effect, divided by 82; this results in a 12.195-KPPS output.

There are three other binary dividers contained in the divider chain; these are a divide-by-19, a divide-by-83, and a divide-by-241. The theory of operation of these binary dividers is the same as the theory of operation for the divide-by-82 configuration.

3.4 TUNED FILTER CIRCUITS

The tuned filter circuits, Figures 3.5, 3.6, and 3.9, are used to multiply the outputs from the four binary dividing circuits by five. That is, they are tuned to resonate at the fifth harmonic of their input frequencies. This multiplication is necessary in generating the 1.002^{+}-kc signal needed to drive the clock at a sidereal rate. The only difference between the tuned filter circuits, except circuits A, D, and F, are the component values. Circuits A, D, and F do not use an amplifier input circuit.

The amplifier is composed of the 2N1132 transistor and associated circuitry which amplifies the 0- and -6-volt input level to 0 and -18 volts for the filter portion. The filter is composed of a resistor and tuned tank circuit. The tank circuit is tuned to resonate at the fifth harmonic of the input frequency, and proper tuning of the tank circuit is critical to the operation of the tuned filter. Final tuning of the tank circuit is accomplished with a trimmer capacitor.

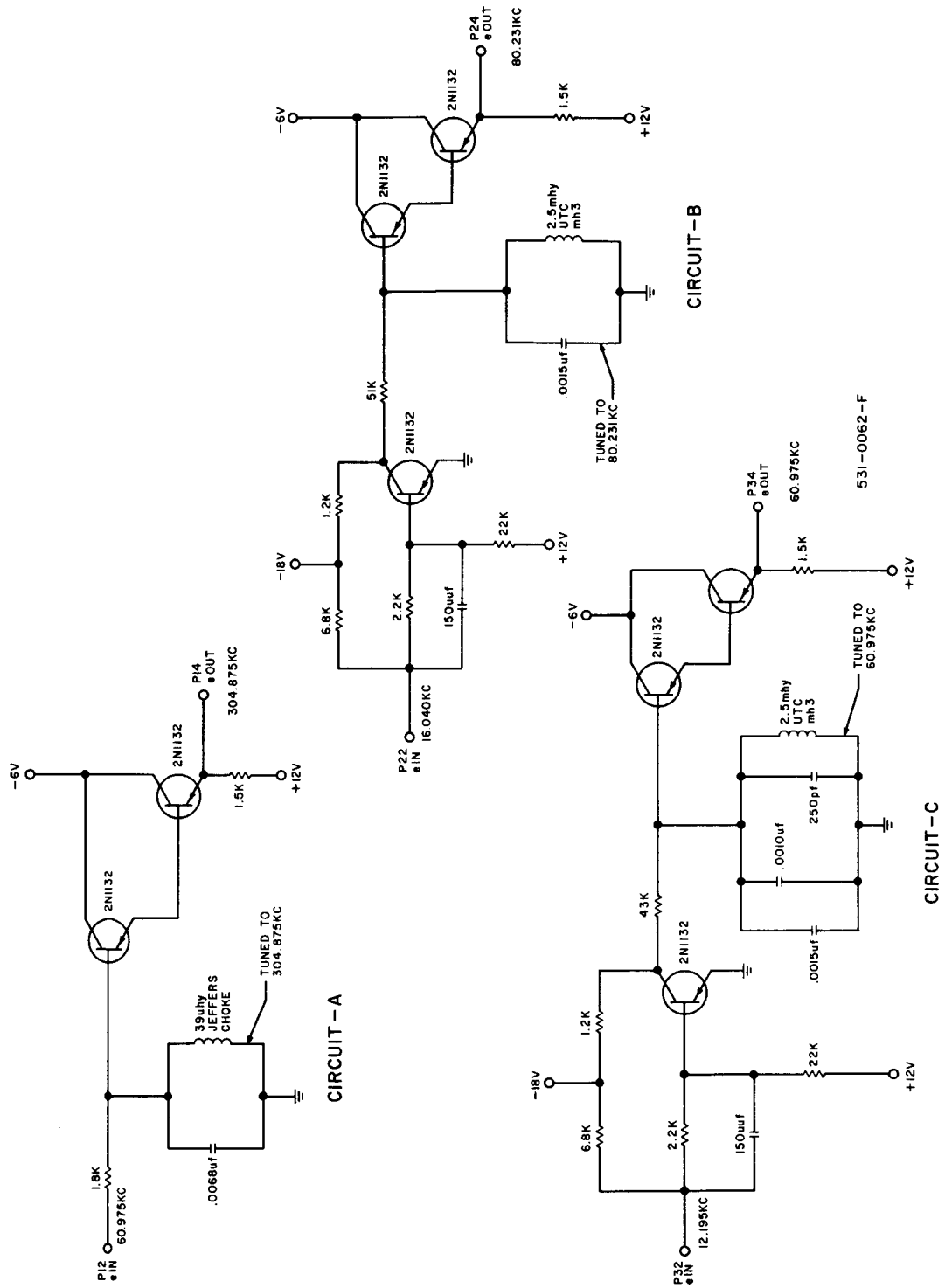


FIGURE 3.5 - TUNED FILTER CIRCUITS, SCHEMATIC DIAGRAMS (CIRCUITS A, B, AND C)

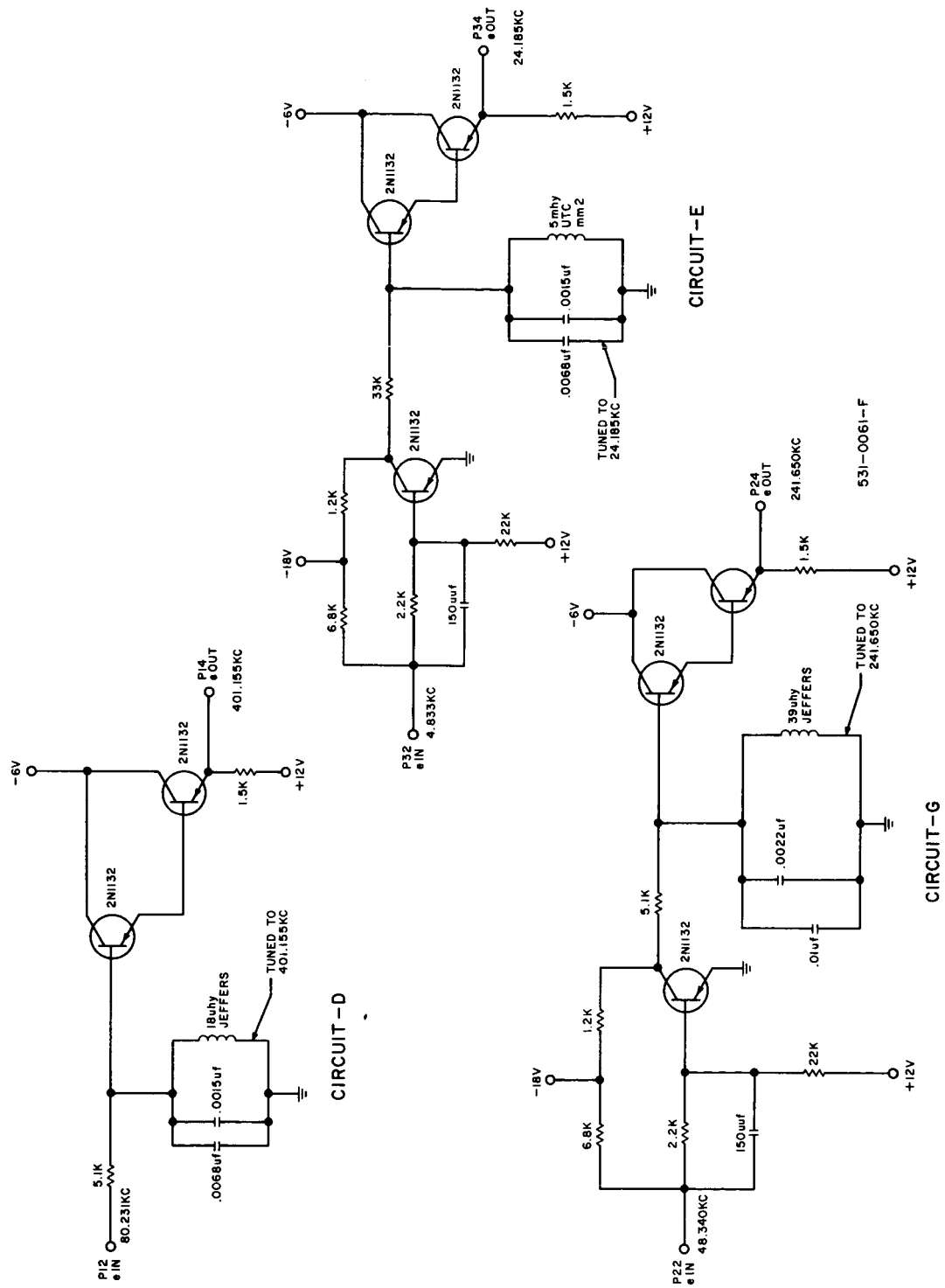


FIGURE 3.6 - TUNED FILTER CIRCUITS, SCHEMATIC DIAGRAMS (CIRCUITS D, E, AND G)

The output from the tuned circuit is applied to the cascaded emitter-follower amplifier circuit composed of two 2N1132 transistors connected in a Darlington emitter-follower configuration. The cascaded emitter-follower amplifier serves as an output buffer and also isolates the tuned circuit and prevents it from being detuned or loaded.

The input signal to tuned filter circuits A, D, and F, is applied directly to the tuned tank circuit.

3.5 TUNED AMPLIFIER CIRCUITS

The tuned amplifier circuits (Figs. 3.7 and 3.8) are used to amplify the resulting fifth harmonic from the tuned filter circuits and to reduce the jitter and ripple and provide a more stable output.

The tuned amplifier contains a collector tank curcuit tuned to resonate at the input frequency.

3.6 FREQUENCY-DOUBLER CIRCUIT

The frequency-doubler circuit, Figure 3.9, is used to multiply or double the 24.165-kc sine wave to correct for the effect of first dividing the 1-Mc signal by 2. The frequency-doubler circuit consists of a full-wave rectifier and a filter circuit tuned to resonate at the second harmonic of the input frequency. The tank circuit is followed by a cascade emitter-follower amplifier and a tuned amplifier.

The frequency multiplication or doubling is accomplished by feeding the 24.165-kc input through the transformer to the full-wave rectifier composed of diodes CR1 and CR2. From the harmonics thus produced the second harmonic of the input is isolated and fed to the tuned circuit composed of capacitors C1 and C2 and the inductor. The output from the tuned circuit, which is the second harmonic of the input frequency or 48.33 kc, is applied to the cascade emitter-follower circuit composed of transistors Q1 and Q2. The cascade

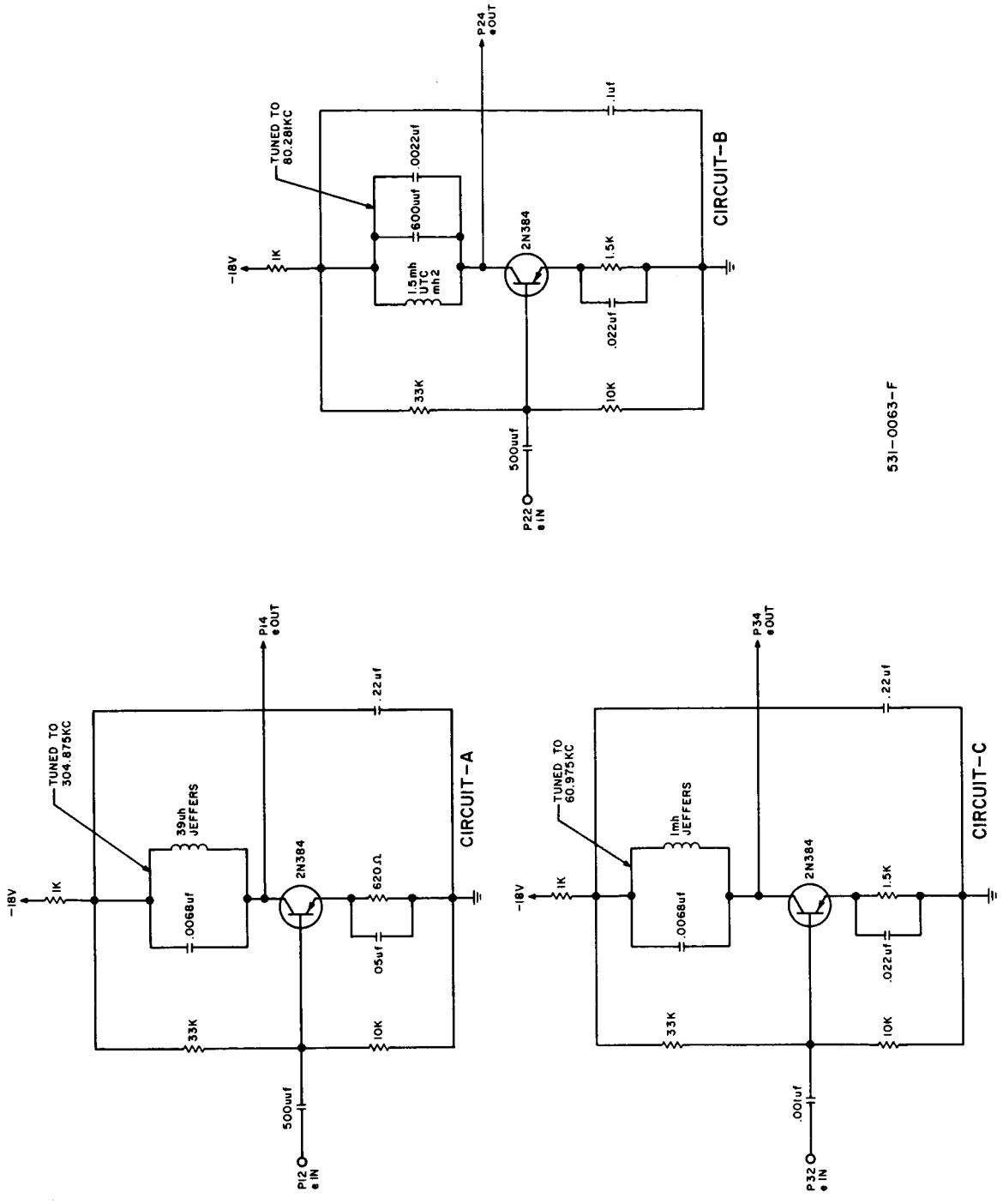


FIGURE 3.7 - TUNED AMPLIFIER CIRCUITS, SCHEMATIC DIAGRAMS (CIRCUITS A, B, AND C)

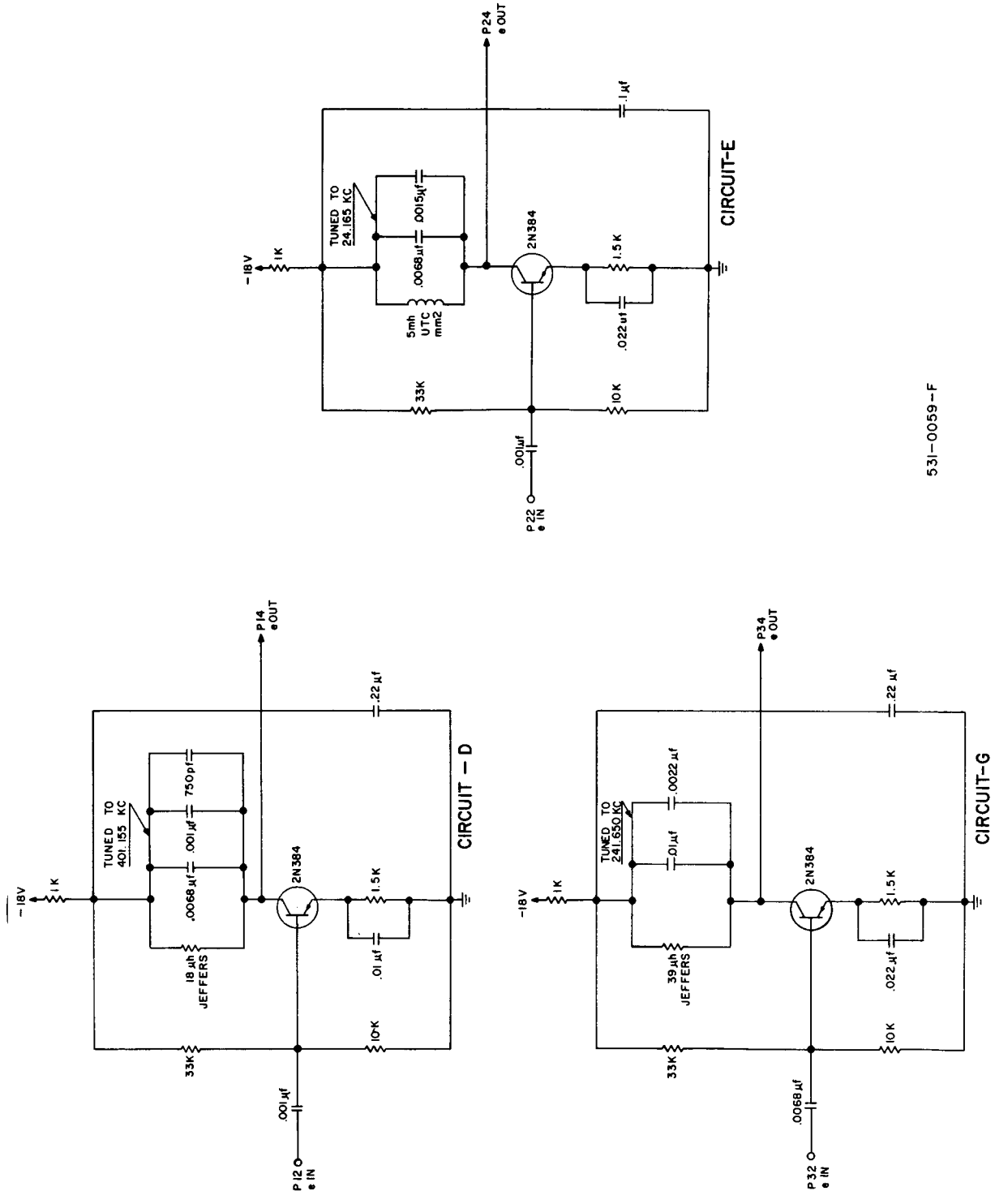


FIGURE 3.8 - TUNED AMPLIFIER CIRCUITS, SCHEMATIC DIAGRAMS (CIRCUITS D, E, AND G)

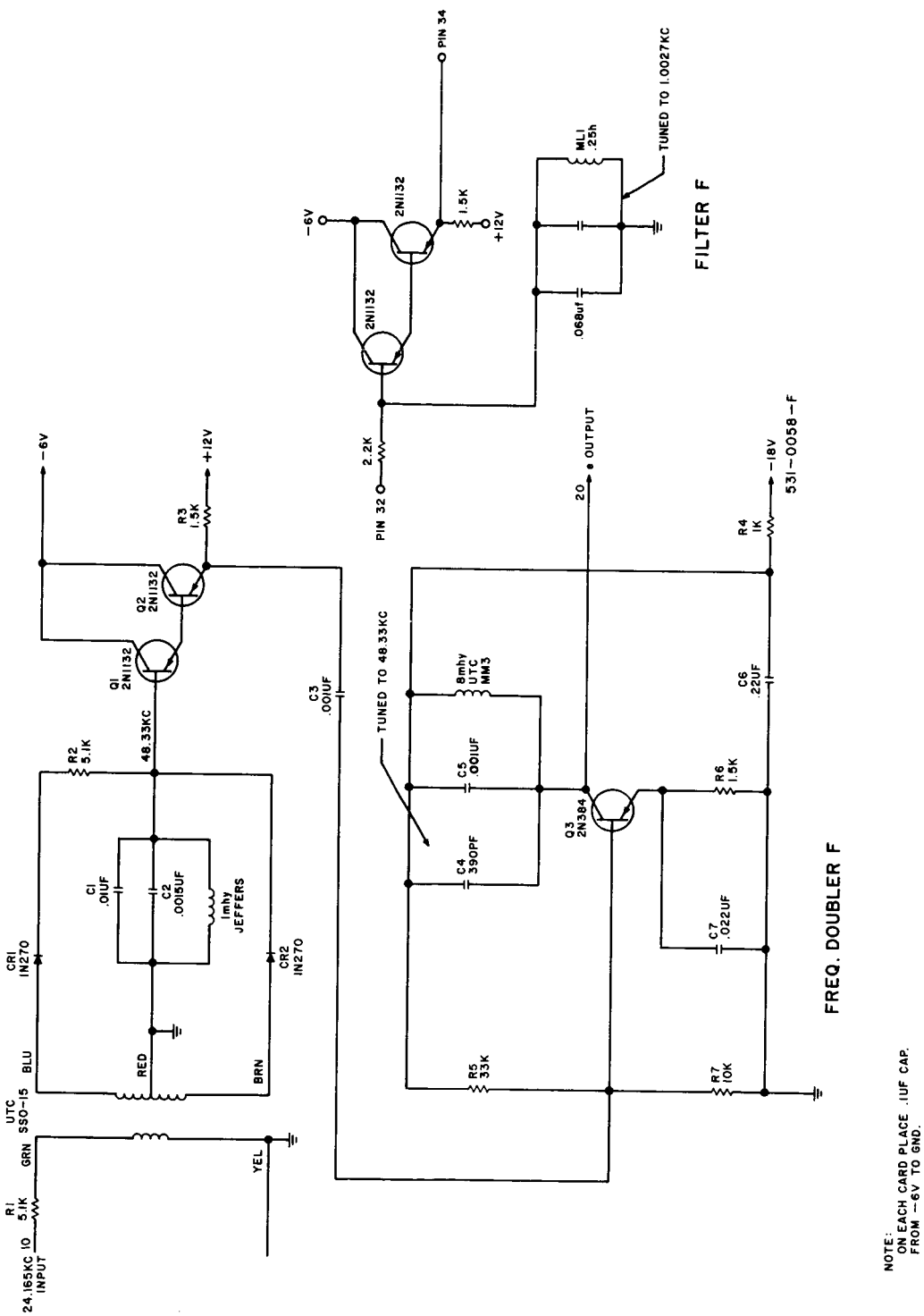


FIGURE 3.9-FREQUENCY-DOUBLER CIRCUIT F AND TUNED FILTER CIRCUIT F SCHEMATIC DIAGRAMS

emitter-follower circuit serves as an output buffer and also isolates the tank circuit and prevents it from being detuned or loaded.

The output from the cascaded emitter-follower circuit is applied through capacitor C3 to the tuned amplifier composed of transistor Q3 and the tuned circuit composed of capacitors C4 and C5 and an inductor. The tuned amplifier eliminates jitter and ripple and provides a highly accurate and stable output.

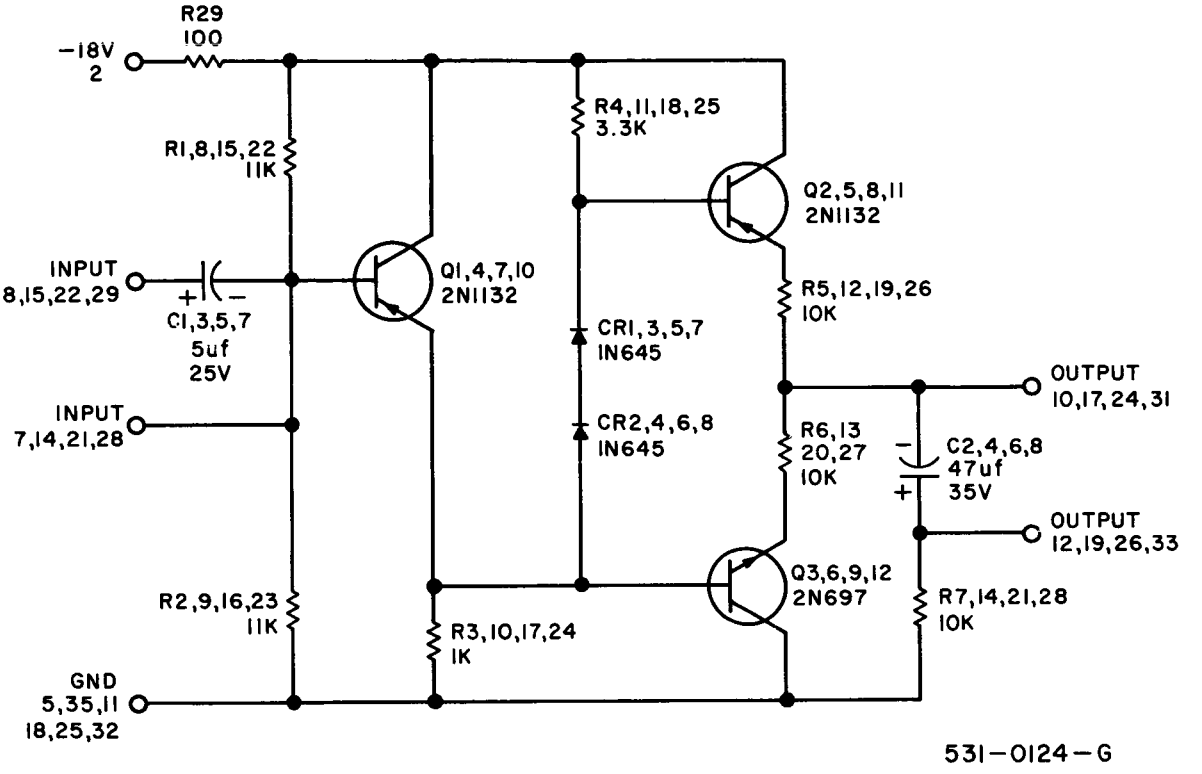
3.7 CABLE DRIVER CIRCUIT (SC-30M)

The cable driver circuit card shown in the schematic diagram of Figure 3.10 contains four identical complementary-symmetry emitter-follower circuits. The input stage is an emitter follower composed of transistor Q1 which presents a high input impedance. The output stage is a complementary-symmetry emitter-follower circuit composed of transistors Q2 and Q3 which are capable of driving low-impedance coax cables (90 ohms) terminated in their characteristic impedance without noticeable distortion. Diodes CR1 and CR2 provide bias for transistors Q2 and Q3 by maintaining a 1.2-volt difference between the bases of the transistors to eliminate crossover distortion.

Transistor Q3 conducts on the positive half of the input sine wave and transistor Q2 conducts on the negative half.

3.8 PHASE-SHIFT RESOLVER

The phase of the 1-kc divider output can be continuously adjusted by turning the TIME REFERENCE - MICROSECONDS dial on the front panel. Turning the dial through a given angle shifts the phase of the resolver output by the same amount. One full turn of the vernier shifts the phase of the 1-kc motor-drive signal by 360^{o} and changes the clock drum position by 1 millisecond, the duration of one period of the 1-kc signal. The 1-PPS TICK and 1-PPS AUXILIARY PULSE outputs are simultaneously shifted by a like amount.



NOTE:

1. ALL RESISTORS 1/4W., ±5%

FIGURE 3.10 - CABLE DRIVER CIRCUIT (SC-30M), SCHEMATIC DIAGRAM

The phase-shift resolver and the rotor angles are shown in Figure 3.11. The phase-shift resolver is a transformer with a rotating primary rotor and stationary secondary stator, which has two perpendicular windings. The output of the resolver circuit (E_{out}) is the vector sum of the voltage induced into each stator (S1 and S2) winding from the rotor (R1) winding. A resistance-capacitance network at the stator output provides a fixed 45° phase lag for the S1 output and a fixed 45° phase lead for the S2 output. Output voltage E_{out} is the vector sum of the phase-shifted S1 and S2 outputs. Turning the rotor increases or decreases the induced voltage in each stator, thus changing the output phase continuously and without limit.

Figure 3.11A shows the resolver in the 0° or no-phase-shift position with a portion of the induced voltage coupled into each stator winding. The resultant output is 0° phase shift.

Figure 3.11B shows the resolver in the +40° position with the rotor winding turned 45° from the 0° reference position. Maximum coupling exists between R1 and S2. The resultant output is +45°.

Figure 3.11C shows the resolver in the -45° (or +315°) position. Maximum coupling exists between R1 and S1 since the windings are parallel. No voltage is induced into S2 since R1 is perpendicular to S2. The resultant output is -45°.

Figure 3.11D shows the resolver in the 135° phase-shift position with the rotor turned 135° from the 0° reference position. R1 and S1 have a maximum coupling and a phase shift of 180° since R1 is inverted. The resultant output is 180° less 45° or 135°.

Figure 3.11E shows the resolver in the 225° phase-shift position with the rotor turned 225° from the 0° reference position. Maximum coupling exists between R1 and S2 since the windings are parallel. R1 and S2 have a phase shift of 180° since R1 is inverted; E_{out} and S2 have an inherent phase shift of 45°. The resultant vector output is the sum of the two phase shifts, (180° + 45°) or 225°.

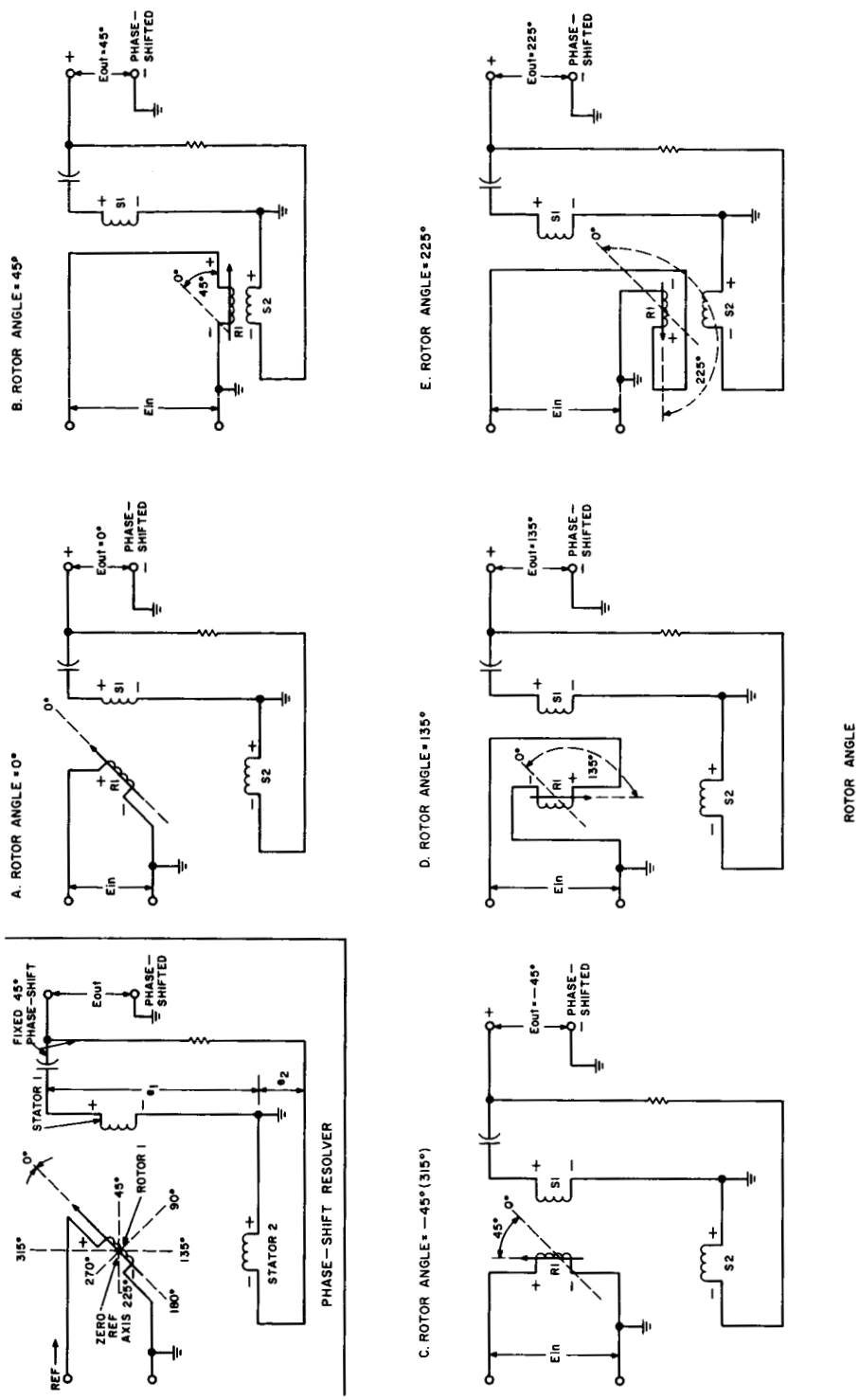


FIGURE 3.11- PHASE-SHIFT RESOLVER AND ROTOR ANGLE, SCHEMATIC DIAGRAMS

3.9 TICK GATE OPERATION (Fig. 3.12)

The circuits described below are located on the A4 pulse generator assembly.

A mechanical light beam interrupter driven by the clock motor allows a light beam to fall on photocell V101 once per second. The photocell output is amplified by Q408 and applied to CR411 and the base of blocking oscillator Q409. Although this positive 1-PPS wavetrain is continuously applied to the base of Q409, it has insufficient amplitude to trigger Q409 into conduction. Phase-shifted 1-kc pips from first blocking oscillator Q407 provide another input; one accurately phased pip is passed each second by the gate. The simultaneous presence of the two pulses drives Q409 into conduction; Q409 provides the external 1-PPS TICK outputs and internally triggers the 100-millisecond multivibrator.

The phase-shifted 1-kc motor drive signals from Q405 and Q406 trigger blocking oscillator Q407 at a 1-kc rate. Diode CR410 clips and limits the 1-kc-pip output to a positive 12 volts. The positive-going phase-shifted 1-kc-pip wavetrain is applied to CR411 and is superimposed with the positive-going 1-PPS wavetrain from the photocell. The presence of the two wavetrains at the base of Q409 drives Q409 into conduction and produces a negative phase-shifted 1-PPS wavetrain at the collector of Q409. The wavetrain is applied directly to the front-panel TICK output connector and is inverted by T404 to provide the positive TICK output at the rear of the chassis and the negative TICK output at the front of the chassis.

3.10 MOTOR AMPLIFIER CIRCUIT

The driver and power amplifier circuits are shown in the schematic diagram of Figure 3.13. The driver circuit accepts the 1-kc output of the resolver and through transformer T401 applies signals of opposite polarity to the bases of transistors Q402 and Q403 so that the resulting outputs on pins 6 and 4 of transformer J103

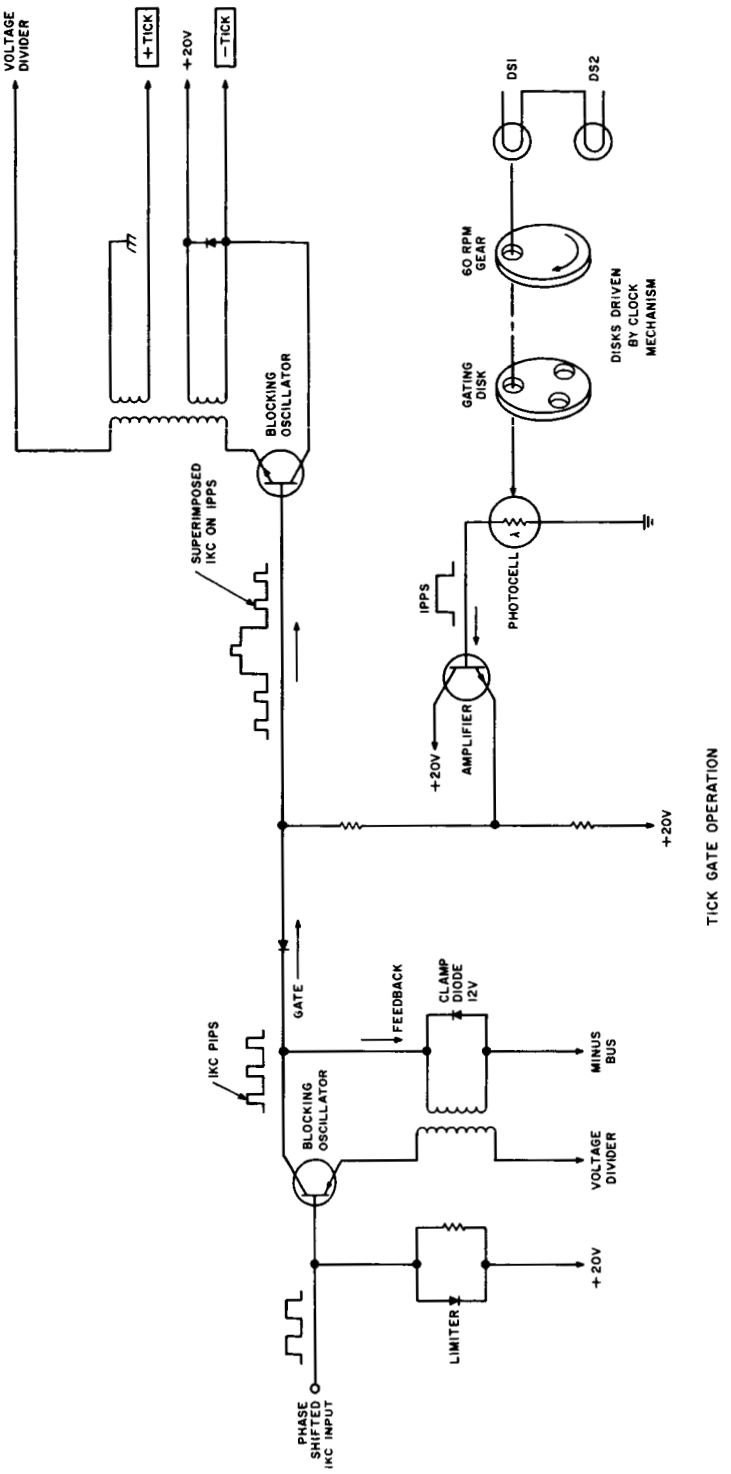


FIGURE 3.12 - TICK GATE OPERATION, PARTIAL SCHEMATIC DIAGRAM

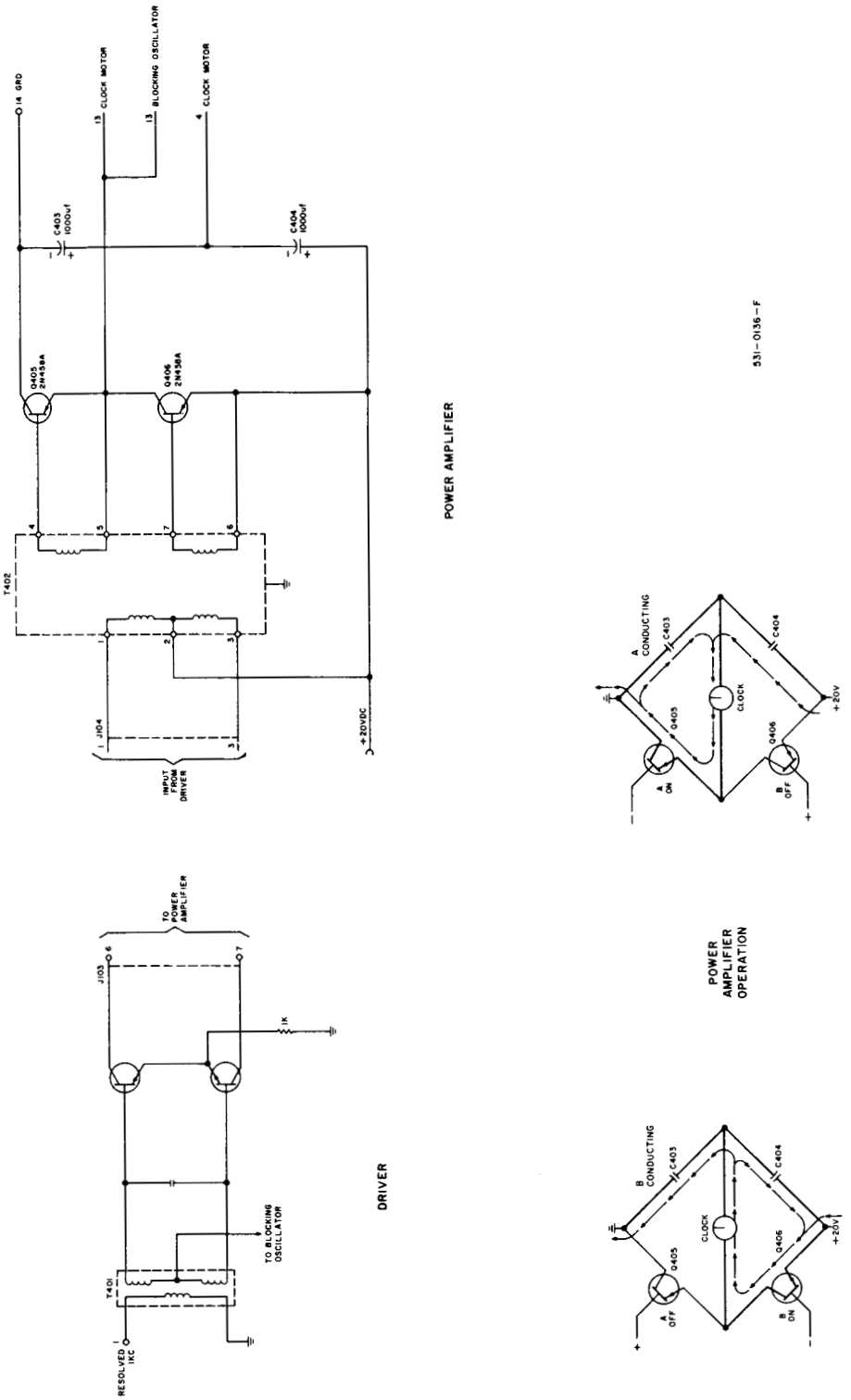


FIGURE 3.13 - DRIVER AND POWER AMPLIFIER, SCHEMATIC DIAGRAM, AND POWER AMPLIFIER OPERATION, FUNCTIONAL DIAGRAM

are 180° out of phase. The phase-shifted outputs of the driver are applied through transformer T402 which provides push-pull drive to bridge connected power-amplifier transistors Q405 and Q406.

The effective path of electron flow is shown at the bottom of Figure 3.13. When transistor Q405 is conducting and transistor Q406 is cut off capacitor C403 discharges and capacitor C404 charges. The electron flow is from left to right through B102. When transistor Q405 is cut off and transistor Q406 is conducting, capacitor C404 discharges and capacitor C403 charges. The electron flow is from right to left through D102.

SECTION 4

TROUBLESHOOTING

4.1 INTRODUCTION

The clock can be slid partly out of the rack (Fig. 4.1) for routine inspection and maintenance while it is operating by pushing the buttons on the front handles. To remove the instrument from the rack, push the button on the slides.

If the operation of the sidereal rate generator is to be continued while it is removed from the cabinet it is necessary to (1) connect a 1-Mc signal to J 113 (BNC connector), and (2) to connect a 115-volt input to J 105.

4.2 TROUBLESHOOTING

In general, the following approach is recommended for finding circuit failures in the sidereal rate generator.

a. Sectionalize trouble by evaluating front-panel symptoms (use Table 2.2).

b. Check the supply voltage and the 1-Mc oscillator. If they are correct, try starting the clock. The clock may have stopped because of a momentary interruption of the supply voltage or the 1-Mc input.

c. Localize trouble by making voltage checks in the defective section.

d. Check for failure of the individual components by substitution, resistance measurements, etc.

e. After determining which section is defective, make dc-voltage checks at the emitter, base, and collector terminals of

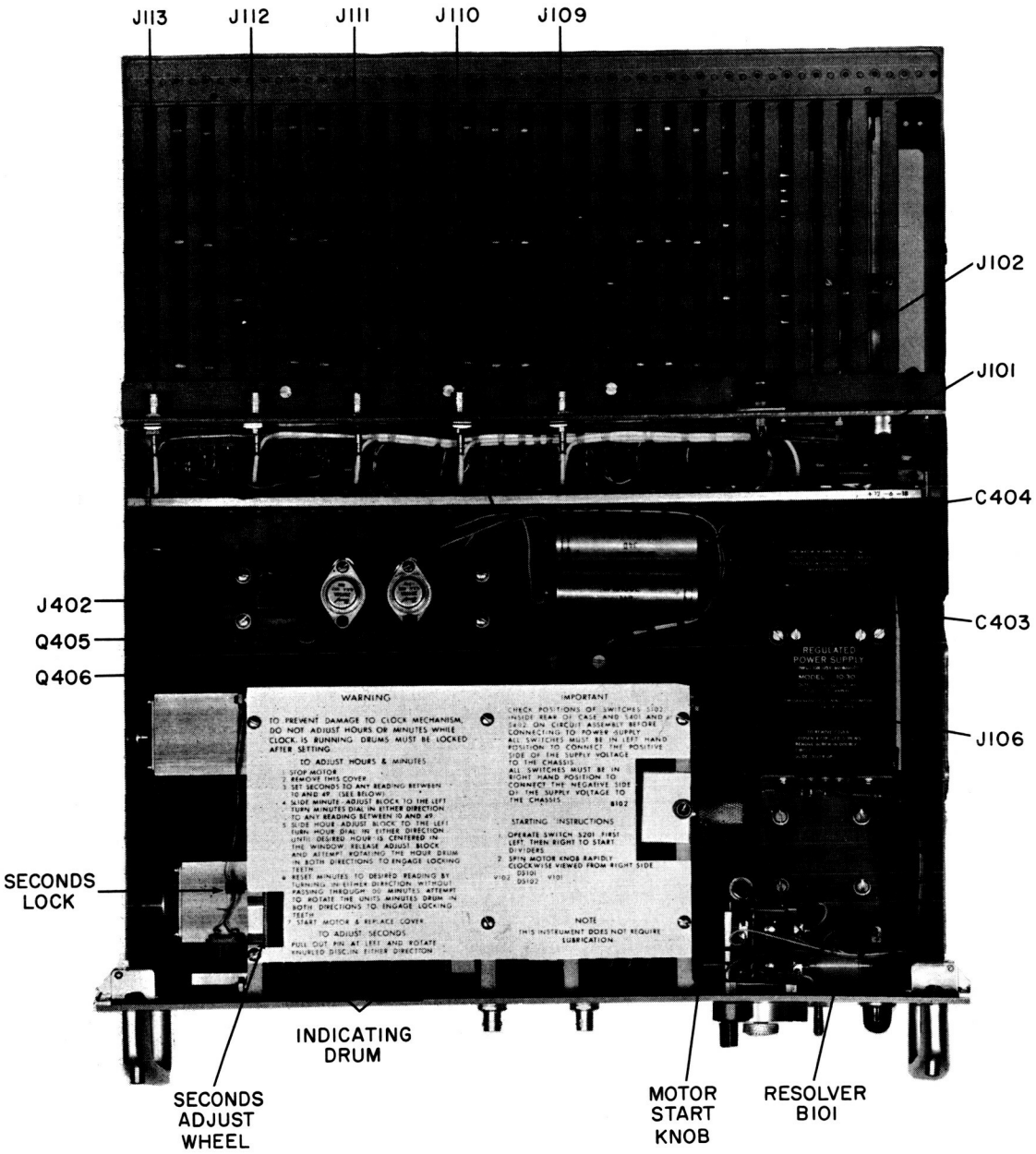


FIGURE 4.1 COMPONENT LAYOUT

each transistor in the defective section.

f. Since the operation of the binary dividers is similar, voltage checks between similar points on each divider can help localize troubles. It may be necessary to use a signal-injection system and a counter and to count the frequencies when trouble-shooting the divider circuits. Be sure that the frequencies agree with those shown in Table 4. 1.

g. Use an oscilloscope and the information contained in Table 4. 1 when checking the operation of the various circuits in the divider chain. Connect a 1-Mc signal to J 113. (See Fig. 3. 2.)

TABLE 4.1 - PERFORMANCE CHECK

Circuit being checked	Signal input	Monitor output at		Output signal
		Pin	Card	
Divide-by-82 circuit	1 Mc	6	3	12.195 k PPS
Tuned filter) Circuit Tuned amplifier) C	12.195 k PPS	34	8, 10	60.975 kc
Tuned filter) Circuit Tuned amplifier) A	60.975 k PPS	14	8, 10	304.875 kc
Divide-by-19 circuit	304.875 k PPS	9	7	16.046 k PPS
Tuned filter) Circuit Tuned amplifier) B	16.046 k PPS	24	8, 10	80.231 kc
Tuned filter) Circuit Tuned amplifier) D	80.231 k PPS	14	11, 15	401.155 kc
Divide-by-83 circuit	401.155 k PPS	9	14	24.165 k PPS
Tuned filter) Circuit Tuned amplifier) E	24.165 k PPS	34 24	11 15	24.165 kc
Frequency doubler	24.165 kc	20	16	48.33 kc
Tuned filter) Circuit Tuned amplifier) G	48.33 k PPS	24 35	11 15	241.65 kc
Divide-by-241 circuit	241.65 k PPS	9	19	1.002+ k PPS
Tuned filter) Circuit F	1.002+ k PPS	34	16	1.002+ kc
Power amplifier PA-30	1.002+ k PPS	8	22	1.002+ k PPS

SECTION 5

TESTING AND ADJUSTMENT

5.1 PERFORMANCE CHECK

Because of its fail-safe circuit design the clock either operates properly or stops completely. Therefore, if the tick-pulse signal occurs regularly once per second it can be assumed that the clock mechanism is operating normally. Check the sidereal 1-kc output to insure that it is 1.002 kc.

5.2 RESOLVER ALIGNMENT

Mechanical alignment of the resolver is not normally required since the resolver output is continuously adjustable. Absolute zero of the resolver and TIME REFERENCE indicator can be obtained with the following alignment procedures:

a. Start the clock. Refer to paragraph 3.2 for starting procedure.

b. With the TIME REFERENCE vernier, set the MILLISECONDS dial to the 00 position.

c. Tighten the LOCK for the TIME REFERENCE control to lock the MILLISECONDS dial to the 00 position.

d. Loosen the three screws holding the resolver to the phase-shift assembly. Screws should be left snug but not tight so that the resolver can rotate.

e. Connect a dual-trace oscilloscope to observe the resolver input (junction C321 and C322) and the resolver output (junction C102 and

and R106) simultaneously. Position the resolver rotor physically so that the input and output signals are in phase.

f. Tighten the resolver retaining screws and recheck the in-phase condition of the resolver input and output signal.

5.3 ALIGNMENT OF LAMPS

The two lamps have three connecting wires; one white wire for each lamp and a black wire common to both lamps. To align the lamps proceed as follows:

a. Disconnect both white wires (if not previously disconnected) from the feed-through insulators. Do not disconnect the black wire (connect to center feed-through if disconnected).

b. Check photocell V101 (located through left motor plate) to verify that the leads (green) are both horizontally positioned and connected.

c. Connect a voltmeter across R415.

d. Rotate the clock motor slowly by moving the 60-rpm drum to the zero position until the (white/black) transition point is aligned with the face-plate zero mark.

e. Connect one of the white wires temporarily to either of the outside feed-through terminals. Adjust lamp mounting assembly by rotating it a few degrees until at least

4 volts dc is measured across R15. Record the voltage reading.

f. Disconnect the white wire connected in step (e) and connect the second white wire to the other outside feed-through terminal. Adjust the lamp mounting assembly by rotating it a few degrees until at least 4 volts dc is measured across R415. Record the voltage reading.

g. Disconnect the lamp wired in step (f); reconnect the lamp used in step (e); voltage across R15 must remain at about 4 volts and the voltage from each lamp should not vary more than $\pm$ 10%.

h. Solder the leads from the lamps permanently to the outside feed-through terminals.

i. Tighten the four setscrews holding the lamp assembly and recheck voltage as in steps (e) and (f). If the voltages have changed and are out of tolerance, loosen two setscrews on the lamp assembly and readjust.